Remarks/Arguments

Claims 1, 5, 6, 9 and 10 have been amended in response to the examiner's objections. It is submitted that these objections have been overcome.

35 U.S.C. §112

The Examiner has objected to claims 1-10 as being indefinite.

Claim 1 has been amended to clarify that the differential value is produced by the subtraction stage. Additionally, the antecedent basis problem with claim 1 on line 13 has been addressed.

Claim 8 has been amended to replace "complete data signal" with "unrectified sampled and digitized ternary data signal." In addition, the path to which the processing or comparison stages correspond to has been clearly identified as the "further path."

It is submitted that the examiner's objections to claim 1 and 8 have been overcome and are in condition for allowance. Such action is respectfully requested.

35 U.S.C. §103

Claims 1-4 and 9-10 stand rejected under 35 U.S.C. §103(a) as being unpatenable over Tanaka et al. (US 5,778,032) in view of Williams (US 5,592,125).

It is submitted that Tanaka et al., does not teach or suggest a phase detector comprising "a delay stage for delaying the digital sample values by one or more sampling clock periods" or "a subtraction stage, to which the undelayed and the delayed digital sample values are supplied to produce a diffcrential value" as recited by the currently amended claim 1.

Tanaka et al. describes a data reproducing method and data reproducing unit. In the embodiment of Figure 7, there is disclosed a sampler 1, a decision circuit 2, a delay circuit 7, a further delay circuit 8, another delay circuit 9, a subtraction stage 13, a multiplication stage 14, a low pass filter 15 and a VCO 6. Without further explanation, the Examiner finds that said delay circuits 7 and 8 corresponds to the claimed delay circuit 52 and the

subtraction stage circuit 13 corresponds to the claimed subtraction stage 53 and the low pass filter unit 15 corresponds to the claimed filter or control stage 60.

It is respectfully submitted that an important difference between the presently invention and Tanaka et al., is that Figure 7 in shows a decision circuit 2 in between the sampling circuit 1 and the delay circuit 7. Said decision circuit 2 alters the complete circuit design in comparison to our claim solution. As shown in Figure 2 of our application, the sample values are forwarded to the delay circuit 52 in their original form, only altered might be the sign of the sample values, which is being done in the rectifier 51. The decision step for converting the sample values into digital data values is done with the processing stage 54 which is positioned behind the subtracting stage 53 in the processing work flow. Therefore, there is no need to add a further decision circuit behind the subtracting stage 13 in Figure 7 of Tanaka et al. In other words the finding of the Examiner is hindsight view, and would not be carried out by the skilled person because he would not have motivation for doing this starting from the circuit design given in Figure 7 of Tanaka et al.

Furthermore, Tanaka et al., teaches the use of a the multiplication stage Fig. 7, 14 multiplies a delayed sample value as an Sn-1 with the difference of delayed and undelayed digital data words generated from the sample values in the decision circuit 2. Tanaka et al., does not teach or suggest the output values fed to the filter unit in the design of the present invention recited in claim 1.

It is further submitted that Williams (US 5 592 125) does not teach a phase detector comprising "a delay stage for delaying the digital sample values by one or more sampling clock periods" or "a subtraction stage, to which the undelayed and the delayed digital sample values are supplied to produce a differential value" as recited by the currently amended claim 1.

The circuit element 123 in Figure 6 of Williams is a buffer, and the only possible input values for this buffer are the logical 1 and logical zero values of gate 121 and gate 122. . (column 6, line 16, line 24, and lines 52 to 59) This shows that the buffer 123 in fact does not assign a decision value to input sample values. To the contrary it assigns a

dedicated voltage to a logical 1 value and another voltage to a logical zero value as described. Therefore, even a combination of both references fails to lead to a construction, as claimed.

It is submitted that neither Tanaka nor Williams teach or suggest the invention recited by the present claim 1. It is therefore submitted that claim 1 is allowable and such action is respectfully requested. Furthermore, since claims 2-10 are dependant on the allowable claim 1, it is submitted that they too are allowable for at least the same reasons that claim 1 is allowable. Such action is respectfully requested.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's representative at (609) 734-6804, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION

I hereby certify that this amendment is being transmitted to the United States Patent and Trademark Office. Fax No. (571) 273-8300.

July 31, 2006
Date

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